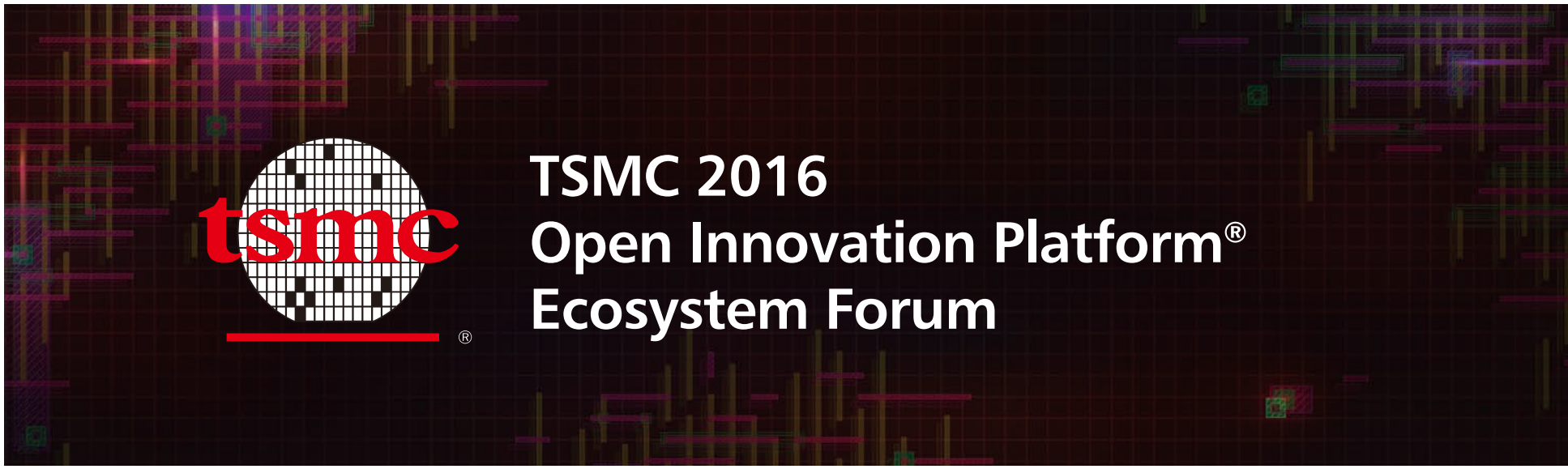
A Game Plan to Deliver OTP in FinFET with New Challenges in Mixed-Signal Physical Design

Kilopass



ABSTRACT

The demand for antifuse one time programmable (OTP) memory in advanced process technologies for security to code storage continues to grow for markets including gaming, mobility, and automotive. The time needed to develop OTP IP or any mixed-signal IP in FinFET is growing, but time-to-market requirements of TSMC and Kilopass customers remain unchanged or are even more aggressive. In this talk, Kilopass addresses methods for delivering OTP IP in FinFET with aggressive schedules to meet our customer's time-to-market requirements. Methods of improving the turnaround time of the development cycle will be discussed. Specifically, challenges of mixed-signal physical design in 10nm and below will be outlined. The talk will conclude with a detailed game plan to tackle challenges from coloring, 1D metal methodology, voltage tagging, and place and route to improve the development turnaround time to meet the time-to-market requirements.

Kilopass

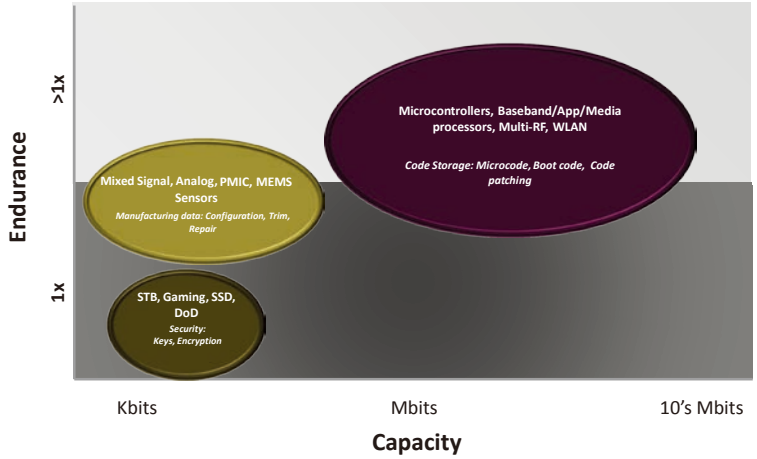
A Game Plan to Deliver OTP in FinFET with New Challenges in Mixed-Signal Physical Design

Jim Mali
Senior Manager, Layout

Kilopass: 15 Years of Memory Experience & Track Record

Anti-Fuse OTP Leadership	Advanced Node Leadership	TSMC License	New OTP Bitcell
80 OTP patents 60 Process Nodes 500 tape-outs (300 @ TSMC)	First to 16nm Leading in 10nm 20 Tape-outs by EOY	10nm & Below Early Bitcell Validation Efficient Distribution	1/10 of Read Power ¼ of Standby Power Simplified Biasing

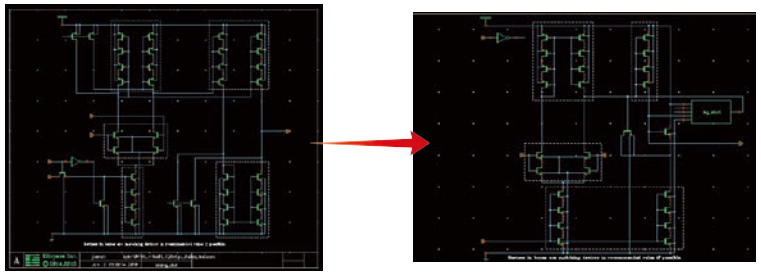
Kilopass Focuses on Three Major Markets



New Process Development at Kilopass

- **Design methodology used at 16nm process nodes were not going to work for 10nm**
- **Complete top down floor plan**
- **No Post layout multi-pattern color engine**
- **Verification intensive**
- **Layout designers to think and draw in 1D with restrictive color requirements**

Design Migration



- **Schematic methodology and Design Migration**
- **Layout first, design second! Schematic was optimized for layout efficiency**
- **Repartition of schematic to help improve layout automation**
- **Extraction of physicals at every cell or block level completion**

Game Plan to Deliver 10nm

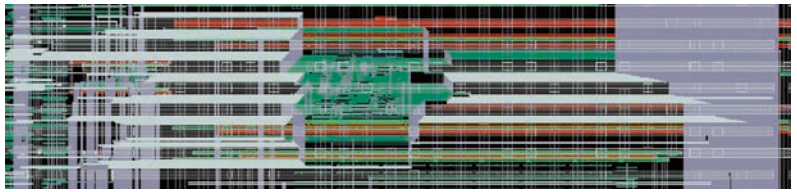
- **Current layout methodology used at 16nm nodes were not going to work**
  - **Game Plan:** Layout designers need to think and draw in 1D with local and global nets
- **Complete Top down floor plan**
  - **Game Plan:** Power grid, route, block placement and transistor placement and connections required. Wire resistance on lower metals required rethinking of local placement
- **All blocks use local interconnections only at metals 2 and 3**
  - **Game Plan:**
    - Local power and routing was restricted to metals 4 and 5
    - With global power in metals 6 and 7
    - Internal block routing was limited to metals 4 and 5
    - Critical signal nets were increased in widths and buffered

New Physical Layouts

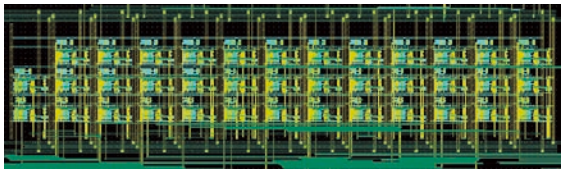
- **Use of TSMC digital standard cells was limited due to routing issues**
  - **Game Plan**- A Kilopass limited internal standard cell library was created to reduce area, boundary effects and increase drive
- **Color at 10nm is a consuming and extensive process**
  - The lack of a post layout engine dictated a extensive color wire floor plan
  - Many revisions and experiments into what was possible given the wire resistances were required
- **CM1 only for type 2**
  - This reduced our usage of TSMC available standard cells. Caused problems with P&R

New Physical Layouts

- **Voltage Tag**
  - **Game Plan:** Tagging the nets manually or with the script
- **Verification**
  - **Game Plan:**
    - Iteration to DRC and LVS
    - Skill coding to fix manual fix voltage, space and color



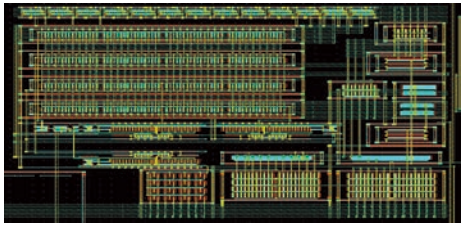
Utilizing Place & Route to Speed up Physical Design



- **Place and Route was used to reduce physical design effort and schedule**
  - This required experiments in digital and analog cells placements, routing and fixed color tracking
  - Mixing of analog and digital blocks, voltages and well potentials
- **Block routing of mixed signal blocks requires a repartitioning of schematics to fully blend in the design**
  - Blocks had a mix of P&R, manual layout and some combination of both
  - Issues required adjusting of base cells and custom scripts
  - Leveraging of these custom methodologies are needed for future processes

Successfully Completed Physical Design in 11 Weeks with Game Plan

- **Met design goals**
- **Met customer delivery schedule**
- **Developed new internal production tools**
- **Created new methodologies for future products**



Kilopass OTP Enablement at TSMC

	Node
tsmc	180G/160G/153G/180BCD
	130G/110G/130LP
	90LP/90G/90GOD/80G
	65LP/55LP/65GP/55GP/55HV
	45LP/40LP
	28 HPM/HPL/HP/LP
	16FF+ (LL,GL)
	10nm and Below (licensed to TSMC directly)

Thank you.

Contact Kilopass for more Information:

Email: info@kilopass.com | 歡迎與我們亞洲辦公室聯絡
電郵: asiasupport@kilopass.com | www.kilopass.com

Kilopass

NOTE